TAMPERE UNIVERSITY OF TECHNOLOGY

Silicon Café:
A Heterogeneous Multi-Processor Platform Based on Coffee (RISC Core)

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Motivation

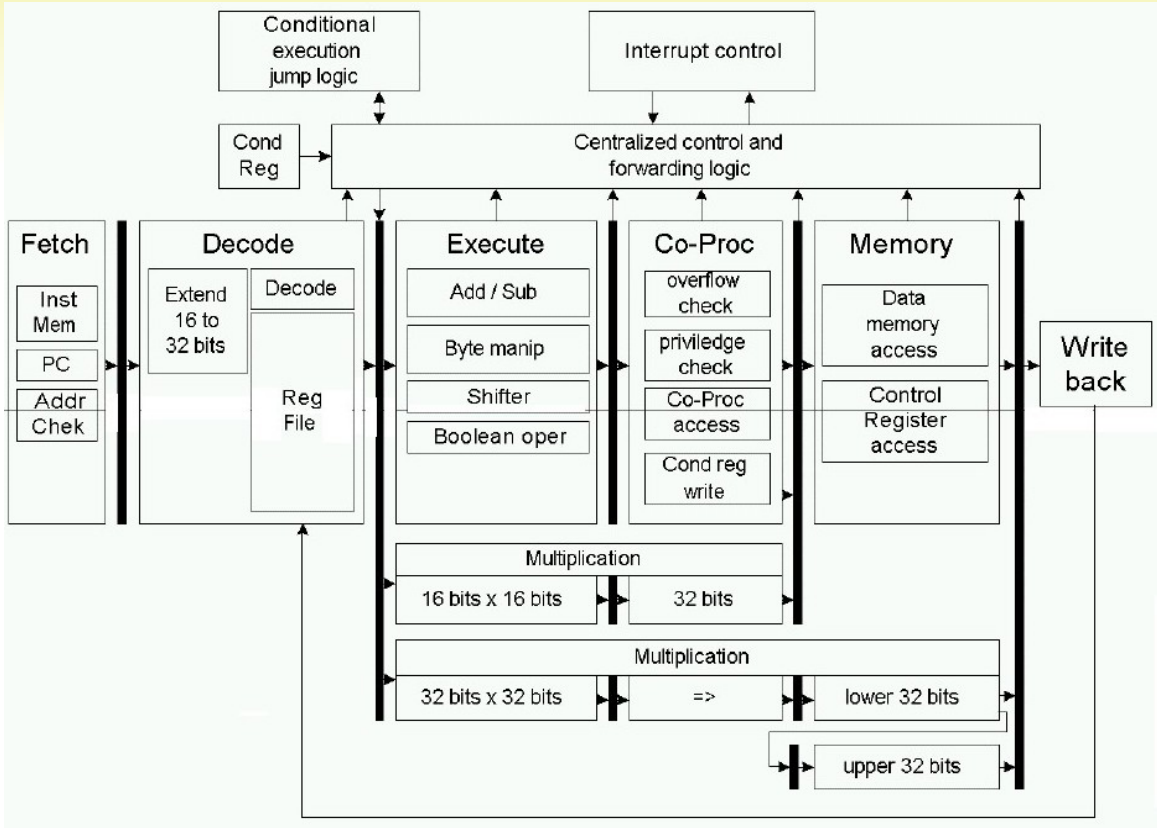
- An efficient platform is needed for a software-defined terminal (SDT)
- SDT requires from the platform efficient joint processing of
  - Receiver baseband algorithms
  - Higher communication layer protocols
  - Multimedia applications
  - = streaming applications distributed on the processing platform
- Also, need to optimize
  - Performance
  - Power consumption

→

- Heterogeneous solution for the hardware platform
  - Different types of processing cores
  - Reconfigurable acceleration hardware
  - Optimized standard blocks
  - Memory
  - High-bandwidth interconnect to support streaming applications

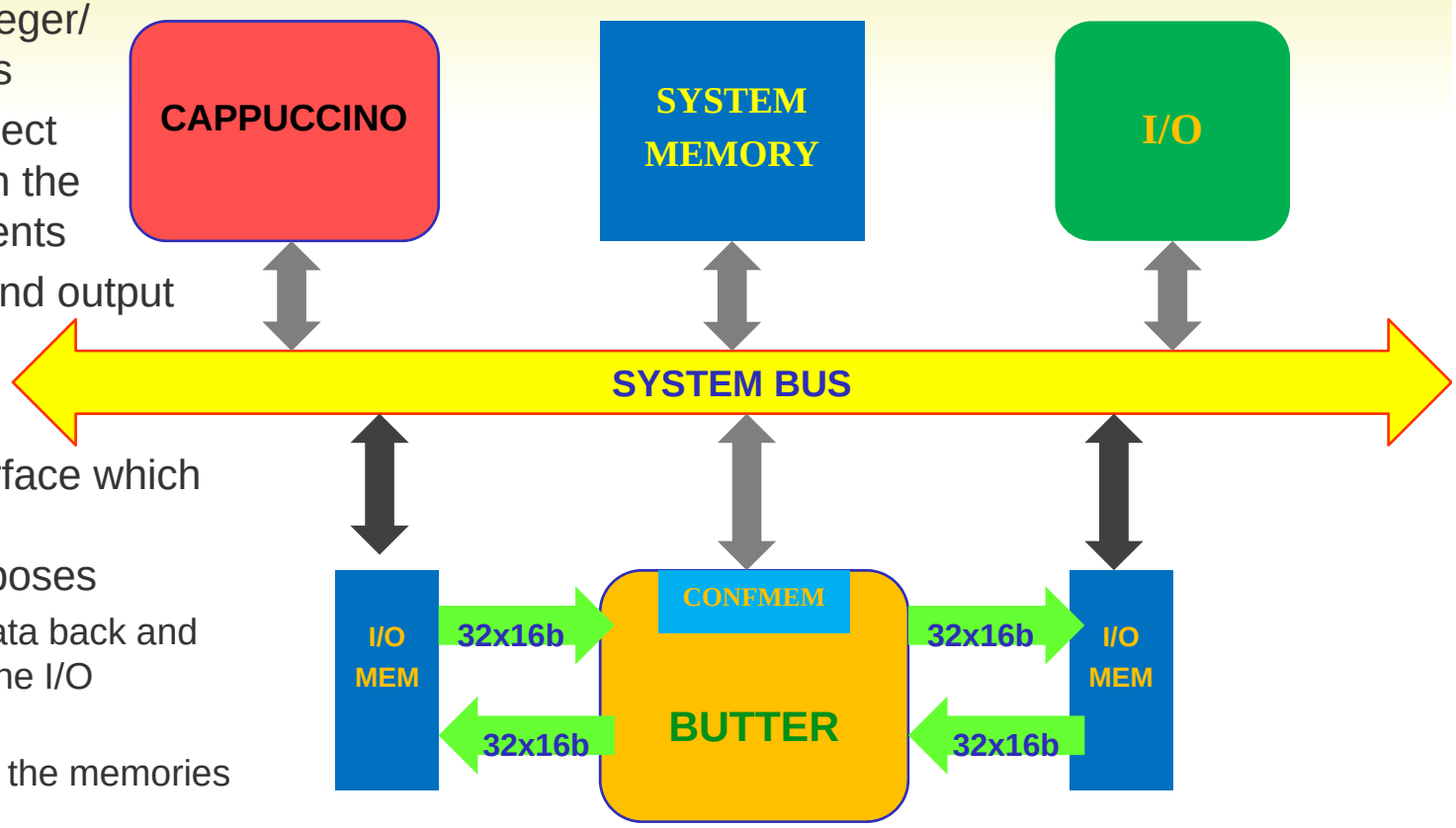
Coffee RISC Core ™

- Open-source RISC core for embedded systems available at **coffee.tut.fi**
- Comes in different flavours
  - ”Regular” Coffee (32-bit integer)
  - Coffee + MILK (FP co-processor)
  - Cappuccino (integer/FP integrated version)
  - Espresso (Coffee accelerated with digital receiver co-processors)
  - Decaf (stripped-down controller)
- Also working on a 2nd generation superscalar Coffee
  - Scalable multi-issue architecture
  - Branch prediction



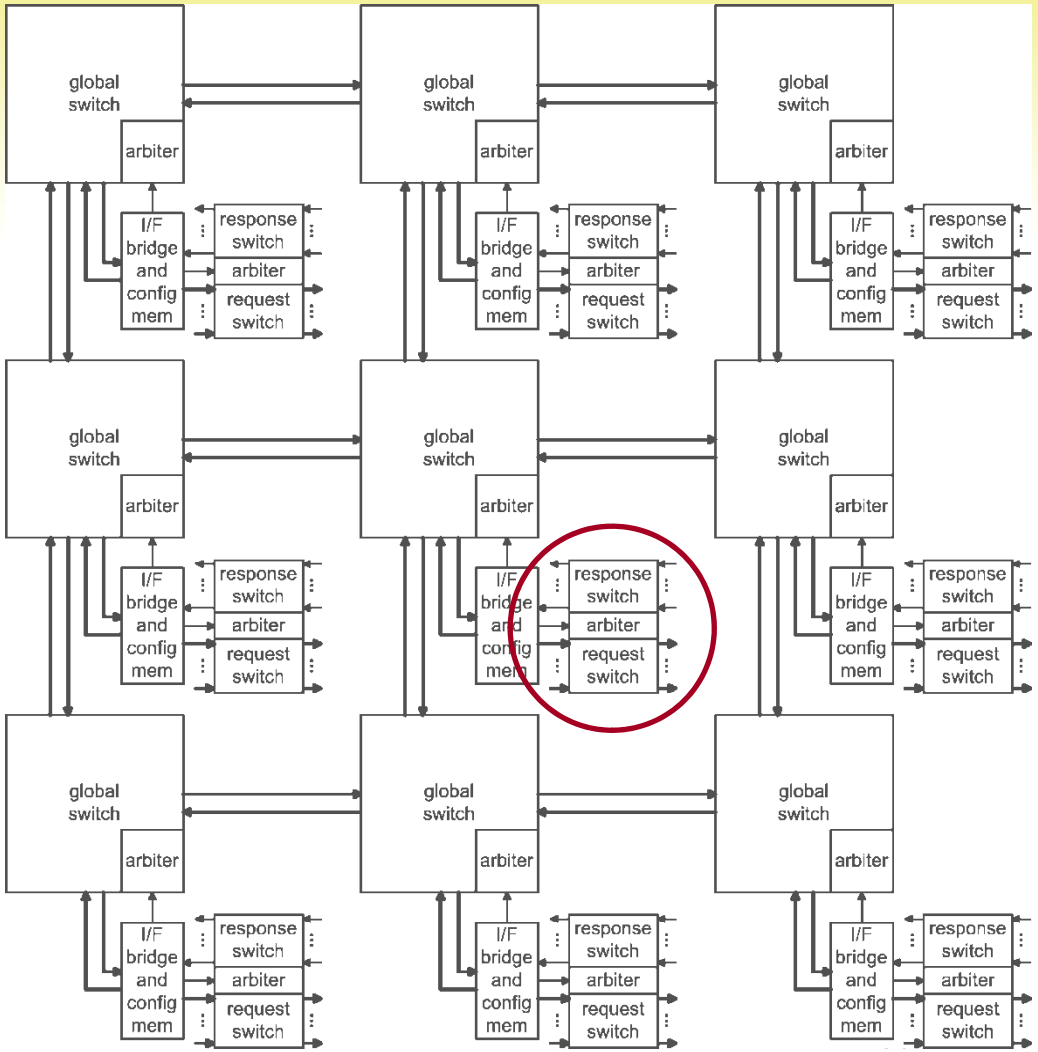
BUTTER Coarse-Grain Reconfigurable Accelerator

- Scalable N x M array of reconfigurable integer/ floating-point units
- Flexible interconnect schemes between the Processing Elements
- Dedicated input and output in addition to the system bus (or network!) interface which is mainly used for configuration purposes
  - Can process data back and forth between the I/O memories
  - DMA to access the memories



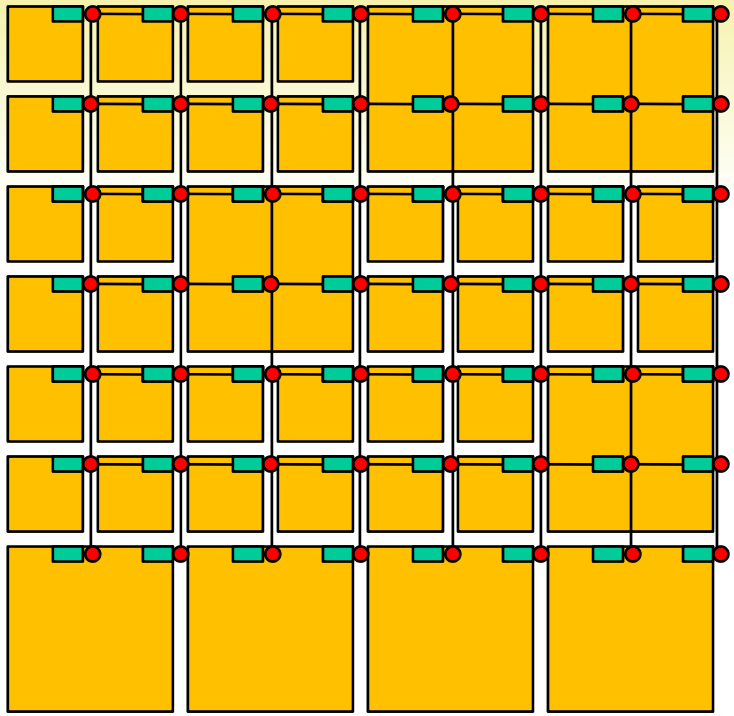
TUT Hierarchical 2nd Generation Network-on-Chip

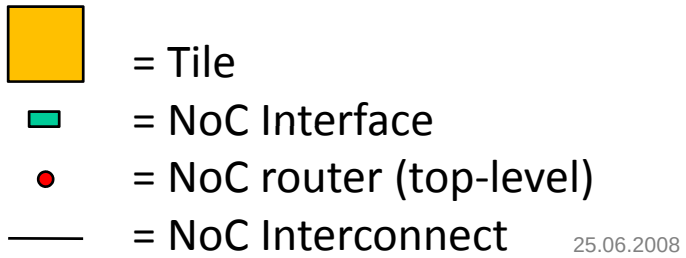
- Local buses replaced by memory-mapped switch cluster
- N masters and M slaves requires N x (M+1) switches
- Bus bottleneck avoided
- Guaranteed service can be provided
- Programmable priority scheme (relative priorities)
- Programmable configuration lifetime and fast context switching (page pointer set externally)
- Pipelined accesses
- Switching delay in 1 ns range in 90 nm technologies, using a few kgates/switch (for 32-bit data)
- Local switches connect to a chip-wide global NoC (Mesh, ring, …)



Silicon Café: Heterogeneous Multi-Processor Platform

- Abuttable tiles of various types
  - Coffee
  - Simplified Coffee (Decaf)
  - INT/FP Coffee (Cappuccino)
  - SuperCoffee (*name???)* of various types
  - Hardwired blocks
  - Reconfigurable blocks
    - Fine grain (eFPGA type)
    - Coarse-grain acceleration (e.g.BUTTER)
  - Common memory buffers
  - Two-level granularity of tiles
- Distributed data memory may be used
  - Remote data managed by DMA, or stall/thread change if ”miss” from local memory
  - Or use L1 caches in some of the tiles and common L2 (or shared main memory)
- Tiles connected by TUT NoC
  - Large tiles may have several NoC I/F
  - Hierarchical NoC (local/global)





Towards Multiprocessor Software-Defined Terminals

- The first Silicon Café platform instance has been designed in VHDL
  (A nine-core Silicon Café = NineSiliCa ??? ☺)
- Starting to map communications and positioning receivers on Silicon Café
- The multiprocessor platforms seen as a unifying architecture for multimedia, outer and inner transceiver, and positioning algorithm execution in future Software Defined Terminals (SDT)
- The processors can also assume the task of determining the services in a cognitive radio type of environment
- However, SDR/CR/SDT is not a solution for all digital receivers: optimized point solutions will remain feasible for cases where the flexibility and versatility of a programmable platform are not needed

Future Plans Regarding Silicon Café

- Need to coordinate and fund a lot of work
  - Further development of platform components (Coffee, BUTTER, etc.)
  - Futher development of compilers and other tooling
  - Implementation (on FPGA board in the first phase)
  - Mapping and benchmarking of applications
- Looking for partnerships, e.g., in
  - Tool development
  - Silicon implementation
  - Applications
- Looking for joint projects to carry on the work
  - EU IST programme projects
  - ARTEMIS
  - Direct bilateral activities
  - Visiting researcher grants
  - you name it…

SoC 2008, Tampere, Finland, Nov. 5-6

Theme of the year: Software-Defined and Cognitive Radio

Tutorial on t.b.d. on Monday November 4

Invited talks

- t.b.d.

Contributed scientific papers

- **deadline June 8, 2008**

Industry track papers

- **deadline August 15, 2008**

Exhibit

Sponsorship opportunities

Steering committee:

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